

FIG. 2

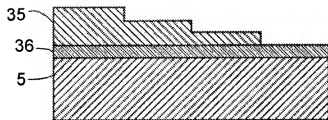


FIG. 3A

A) PATTERNING OF
THE AS-GROWN
WAFER

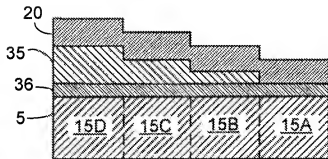


FIG. 3B

B) PATTERNING OF THE
AS-GROWN WAFER,
DIELECTRIC CAP
DEPOSITION AND RTA



FIG. 3C

C) REMOVE ALL
SACRIFICIAL LAYERS FOR
FURTHER PROCESSING
OF THE DEVICE WAFER


DEVICE
WAFER


SACRIFICIAL
LAYER


ETCH
STOP


DIELECTRIC
CAP

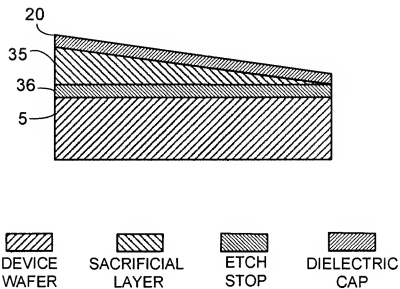


FIG. 4

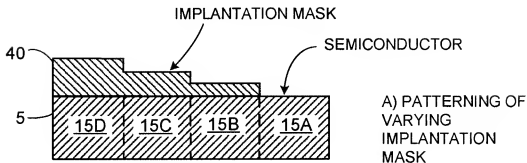


FIG. 5A

IMPLANTATION FLUX (UNIFORM DOSAGE & ENERGY)

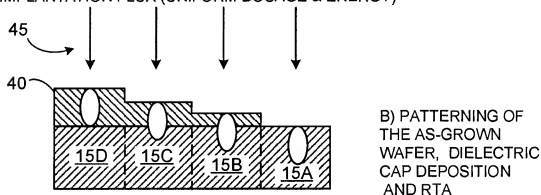


FIG. 5B

LEFT-OVER IMPLANTATION DAMAGE IN SEMICONDUCTOR

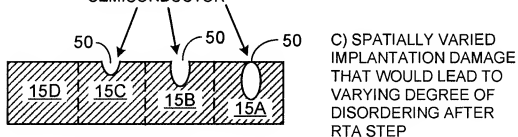


FIG. 5C

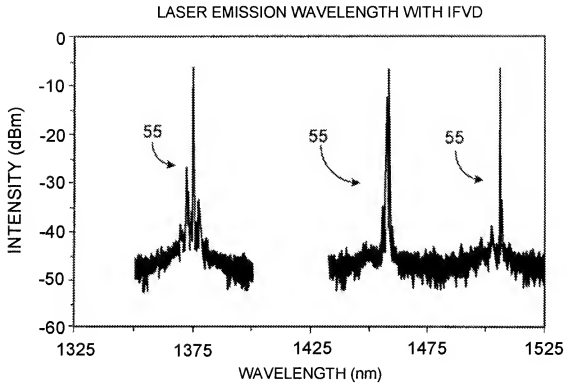


FIG. 6

